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# Activation energy of drain-current degradation in GaN HEMTs under high-power DC stress

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ABSTRACT

We have investigated the role of temperature in the degradation of GaN High-Electron-Mobility-Transistors (HEMTs) under high-power DC stress. We have identified two degradation mechanisms that take place in a sequential manner: the gate leakage current increases first, followed by a decrease in the drain current. Building on this observation, we demonstrate a new scheme to extract the activation energy ($E_a$) of device degradation from step-temperature measurements on a single device. The $E_a$'s we obtain closely agree with those extracted from conventional accelerated life test experiments on a similar device technology.



## 1. Introduction

In the last few years, high-voltage GaN FET technology has burst into the scene promising to revolutionize high-power high-frequency amplifiers as well as high-voltage power management systems [1–6]. A critical concern with this new technology is reliability [7–15]. This is particularly problematic due to the absence of a native substrate for GaN.

In this work, we study the role of temperature in the degradation of GaN HEMTs biased under high-power conditions, a topic that, in contrast with the OFF-state, has received little attention in spite of its importance for power amplifier applications. A key difficulty in high-power stress experiments is managing self-heating and carrier trapping which is temperature dependent [16,17]. Unless these issues are correctly handled, it is difficult to isolate the dominant degradation mechanism and obtain its activation energy ($E_a$). This is required before device lifetime projections to realistic operating conditions can be made. Deriving the $E_a$ of degradation in particular is very time consuming as it requires long-term stress experiments in many devices. In the early stages of development of a new technology, this is also difficult as variations in device characteristics introduce significant ambiguity in the interpretation of the results.

We present here a new methodology to study the high-power degradation of GaN HEMTs. Our approach is based on *step-temperature experiments* in which constant electrical stress is applied at a certain temperature for a given length of time and periodically the temperature is increased in steps. In this way, and with appropriate care to minimize the effect of trapping, we show that the activation energy of the dominant degradation mechanism can be derived from measurements *on a single device*. The new technique that we propose here, while demonstrated under high-power stress conditions in GaN HEMTs, should be applicable to other regimes of operation and other devices. Our research also reveals a sequential degradation pattern for the gate and drain currents in a GaN HEMT under high-power bias at high temperature in long-term stress experiments. Gate current degradation takes place first. Only after the gate current increase has saturated, drain current degradation occurs in a temperature-activated manner.

This paper is an augmented description of the presentation made in [18].

## 2. Experiments

The devices used in this study are prototype packaged S-band single-stage MMICs using a GaN-on-SiC HEMT. The transistor features $L_g = 0.25$ μm and $W_g = 2 \times 280$ μm.

Testing is carried out in an Accel-RF life-test system equipped with a switching matrix that allows device characterization through external test equipment [19]. A flow chart of a typical step-temperature experiment is shown in Fig. 1. At its heart, the device is stressed for some time at high power and at a set base-plate temperature, $T_{stress}$. After a certain stress time, we interrupt the stress, lower the base-plate temperature to 50 °C and characterize the device. We call this the "inner loop." After a number of

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"inner loops" have been repeated, we detrap the device through an in-situ bake at 250 °C for 7.5 h, carry out a detailed characterization at 50 °C, increase to a higher $T_{stress}$ and resume the high-power stress at this new base-plate temperature. We denote this the "outer loop." Through detailed experiments, we have determined that the 250 °C baking results in nearly complete device detrapping without introducing any significant degradation. This allows us to evaluate permanent device degradation, free of carrier trapping effects. Other detrapping methods commonly used such as visible or UV light illumination [20,21], are not available as these are packaged devices.

In our study, we focused on the degradation of the maximum drain current, $I_{Dmax}$ (defined at $V_{DS}$ = 5 V, $V_{GS}$ = 2 V), and the drain resistance, $R_D$ (defined as the extrinsic resistance on the drain side measured at 20 mA/mm using the gate current injection technique [22]). These figures of merit have been found to correlate most closely with RF power degradation [19,23,24]. Other figures of merit, such as $R_S$ and $I_{Goff}$ are also tracked. $R_S$ is defined as the extrinsic resistance on the source side measured at 20 mA/mm using the gate current injection technique. $I_{Goff}$ is defined as the gate current at $V_{DS}$ = 0.1 V and $V_{GS}$ = −5 V. We have verified that repeated measurement of these figures of merit under the selected conditions is "benign" and produces minimum changes in the device characteristics.

Device thermal models provided by the manufacturer in combination with an assessment of the electrical power supplied to the device are used to estimate the channel temperature during stress, $T_{channel}$.

## 3. Results

Typical results are shown in Fig. 2. Here, the device is stressed at $V_{DSQ}$ = 40 V, $I_{DQ}$ = 100 mA/mm with $T_{stress}$ increasing from 50 °C to 230 °C for various lengths of time. We observe that the off-state gate current $I_{Goff}$ increases by about 3 orders of magnitude starting at $T_{stress}$ = 170 °C and saturating at $T_{stress}$ = 190 °C (Fig. 2a) [10,12]. The maximum drain current $I_{Dmax}$ starts to decrease at $T_{stress}$ = 190 °C. By the time the device blows up at $T_{stress}$ = 230 °C ($T_{channel}$ = 330 °C), $I_{Dmax}$ has decreased by about 80%. $R_D$ follows a degradation pattern that tracks that of $I_{Dmax}$ (Fig. 2b). $R_S$ exhibits much less degradation, as is commonly observed [25].

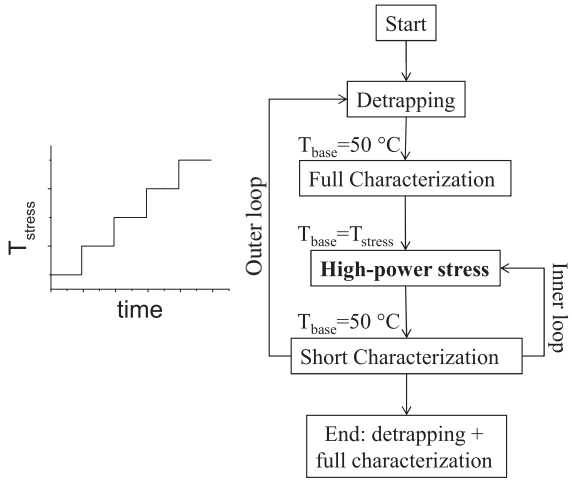


**Fig. 1.** Left: schematic of temperature evolution of the step-temperature stress experiments performed in this study. Right: flow chart of a typical experiment. A detrapping step brings the device to a reproducible detrapped state to assess permanent degradation. The device is stressed for a length of time and regularly characterized in an "inner loop". The stress temperature is stepped up periodically as the experiment flow goes through the "outer loop".

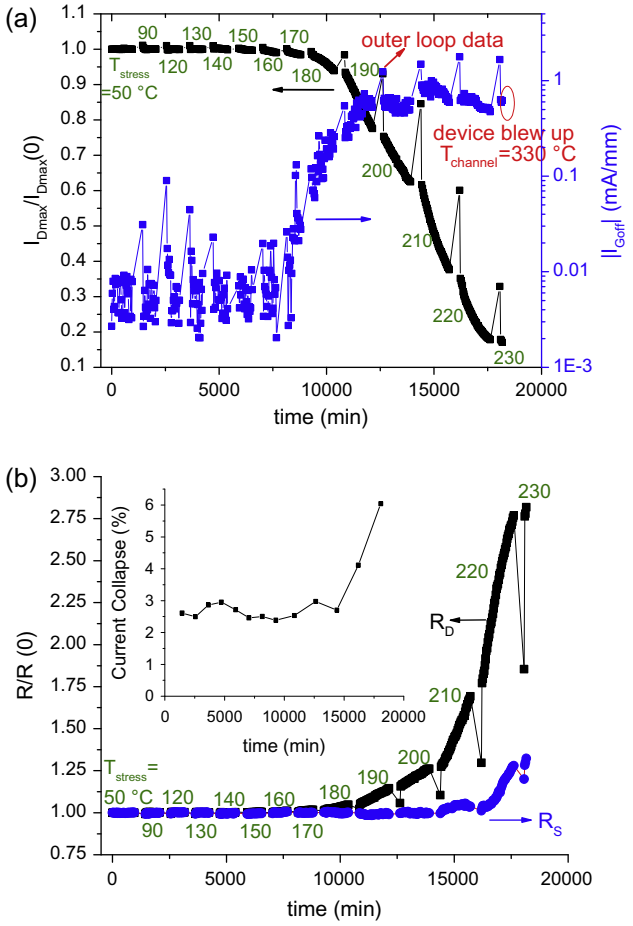


**Fig. 2.** Evolution of degradation of (a) normalized $I_{Dmax}$ (defined @ $V_{DS}$ = 5 V, $V_{GS}$ = 2 V) and $|I_{Goff}|$ (defined @ $V_{DS}$ = 0.1 V, $V_{GS}$ = −5 V), (b) normalized $R_D$ and $R_S$. Both outer loop and inner loop data are included in the graphs. Inset: current collapse measurements in the outer loop. The device was stressed at $V_{DSQ}$ = 40 V and $I_{DQ}$ = 100 mA/mm at a base temperature that increases from 50 °C up to 230 °C.

There is a marked difference between inner loop data (most of the data points) and outer loop data (those sticking out between different stress temperature steps) which are measured with the device freshly detrapped. Outer loop data reflects permanent damage while inner loop data also includes the effect of trapping. The difference between these two sets of data dramatically illustrates the impact of trapping. As is well known, electron trapping produced by high-voltage stress results in a reduction in the drain current of a HEMT due to a lowering of the sheet carrier concentration in the extrinsic drain close to the gate. Less known is the fact that electron trapping also reduces the HEMT gate current as the electric field at the edge of the gate is mitigated [21]. The data of Fig. 2 is consistent with a device that suffers considerable trapping in the inner loop but is detrapped in the outer loop.

Evidence of trapping can also be seen from in-situ current collapse measurements that we perform in the outer loop immediately after device detrapping (inset of Fig. 2b). Current collapse in GaN HEMTs is a temporary reduction of drain current immediately after the application of high voltage [26–28]. A conventional technique to assess current collapse relies on short-pulse characterization of the device. Here, we have adopted a relatively long pulse technique which can be carried out in standard DC characterization equipment and is amenable to integration with long-term stress experiments [29]. In this technique, with a device freshly detrapped and under $V_{DS}$ = 0 conditions, a pulse of −10 V is applied to the gate for 1 s. This often triggers enough electron trapping for

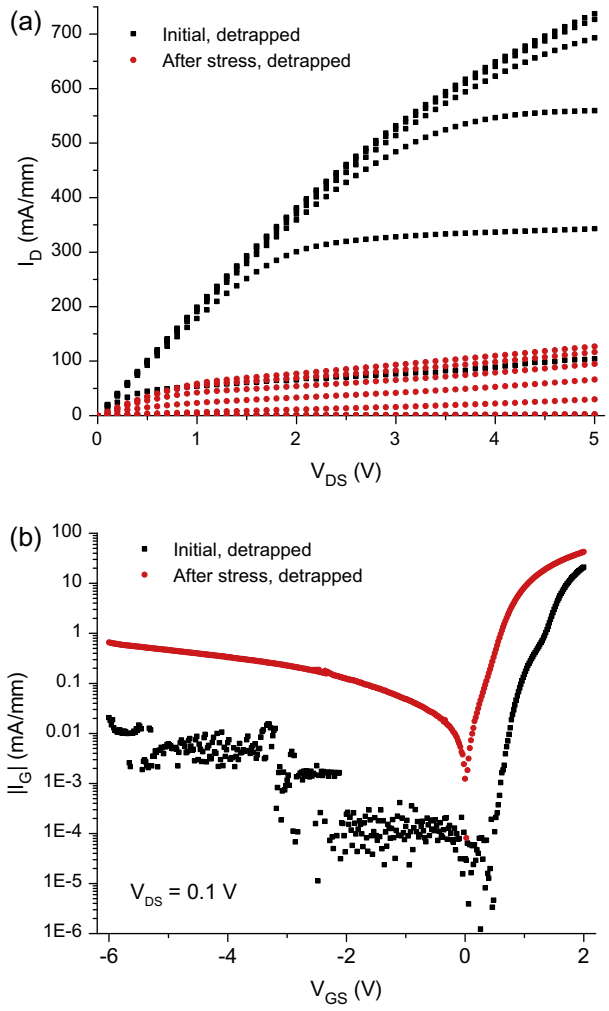


**Fig. 3.** (a) Output characteristics and (b) transfer characteristics of detrapped device of Fig. 2 before stress and after $T_{stress}$ = 220 °C stress.

a sufficient length of time to be observable with the millisecond-type measurements that are possible using DC characterization tools. By measuring the maximum drain current $I_{Dmax}$ immediately before and after the $V_{GS}$ pulse, current collapse can be evaluated as the percentage change in $I_{Dmax}$. The evolution of current collapse in our experiment, as seen in the inset of Fig. 2b, is quite typical of stress experiments in GaN HEMTs [10,15,30]. The virgin device suffers from a certain degree of trapping associated with the surfaces, crystallographic defects or other imperfections that are inevitably present. Under high temperature stress conditions, additional defects are introduced that increase the current collapse suffered by the device. In the case of the data of the inset of Fig. 2b, this is seen to occur after high-power stress at 220 °C.

Detrapped output and gate characteristics of the device of Fig. 2 in its virgin state and right after stress at $T_{stress}$ = 220 °C are shown in Fig. 3. The change in the output characteristics indicates a degradation of more than 65% in the drain current. Since in both cases the measurements are obtained right after the device is properly detrapped, the observed change in characteristics reflects permanent degradation, free of carrier trapping effects. An increase of the gate current of more than two orders of magnitude is also observed. The severe degradation that we have been able to impose on this device enables us to study the temperature dependence of the degradation rate and extract its activation energy.

In the analysis of stress experiments, it is often assumed that for short times the degradation rate is linear in time and thermally activated with a rate constant that follows Arrhenius law:

$$k = Ae^{-E_a/k_BT} \tag{1}$$

Here, $A$ is a pre-exponential factor, $k_B$ is Boltzmann constant, and $E_a$ and $T$ are the activation energy and temperature, respectively. According to this, we can write

$$\ln\left(\frac{1}{|slope|}\right) = E_a\left(\frac{1}{k_BT}\right) + C \tag{2}$$

where *slope* is the rate of change of the physical variable of interest.

Following this approach, Fig. 4 shows Arrhenius plots for the rate of degradation of $I_{Dmax}$ and $R_D$ obtained from the inner and outer loop data. Using the inner-loop data, the activation energy for $R_D$ is almost twice as large as that for $I_{Dmax}$. The relatively large discrepancy between the two $E_a$'s is mainly due to the complications introduced by trapping related degradation. Since traps exist in different energy levels as well as different positions inside the heterostructure, it is hard to interpret the activation energies obtained from data that mixes trapping-related as well as

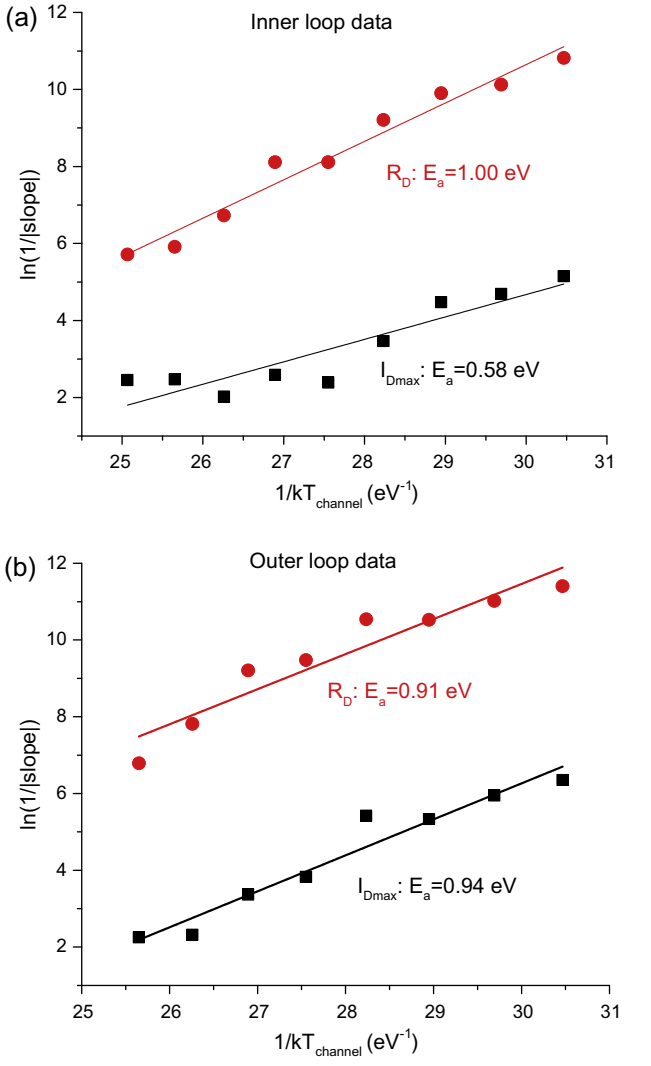


**Fig. 4.** Arrhenius plot for rate of permanent degradation of $I_{Dmax}$ and $R_D$ extracted from data collected (a) every 20 min during stress (inner loop data) and (b) after the detrapping step that follows each temperature stress period (outer loop data) for the experiment of Fig. 2.

permanent degradation. What is more, trapping and detrapping of electrons happen at different rates under different stress temperatures, making it hard to interpret $E_a$ for trapping related degradation in a consistent way.

These problems motivate us to study the outer loop data which reflects permanent device degradation only. In Fig. 4b it is clear that the degradation rates of both $I_{Dmax}$ and $R_D$ are thermally activated. We furthermore obtain $E_a$ values for $R_D$ and $I_{Dmax}$ degradation that are very close to each other, reflecting the same underlying degradation physics. The close correlation between $R_D$ and $I_{Dmax}$ degradation is not universal but has been observed in multiple experiments in a variety of devices [25].

Similar experiments were carried out on other samples. In some devices, we did not observe significant $I_D$ degradation before they blew up. An example is shown in Fig. 5 for a device that was stressed at $V_{DSQ}$ = 40 V and $I_{DQ}$ = 100 mA/mm with $T_{stress}$ increasing from 50 °C to 220 °C (600 min/step).

Unlike the example of Fig. 2, the off-state gate current $I_{Goff}$ does not increase in a significant way throughout the experiment. The maximum drain current $I_{Dmax}$, also shows very small overall degradation. Consistent with the evolution of $I_{Dmax}$, the drain and source resistances also suffer negligible degradation. Under these conditions, it is not possible to extract the activation energy of the device degradation rate using our proposed procedure.

The reason for the uneven degradation behavior observed in different devices is not clear. The fact that in Fig. 5 the total experiment lasted shorter time than that of Fig. 2 is not believed to be a significant factor. The stress time that matters most is that in which the device is at a baseplate temperature above ~190 °C. In both experiments, the stress time with the device above this temperature is rather similar.

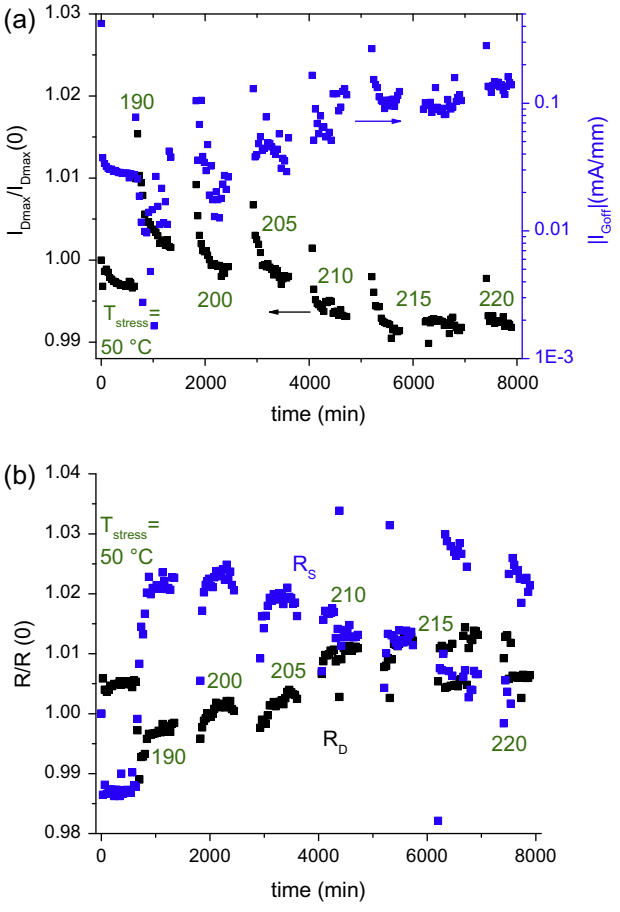


**Fig. 5.** Evolution of degradation of (a) normalized $I_{Dmax}$ and $|I_{Goff}|$ and (b) normalized $R_D$ and $R_S$. Both outer loop and inner loop data are included in the graphs. The device was stressed at $V_{DSQ}$ = 40 V and $I_{DQ}$ = 100 mA/mm at a base temperature that increases from 50 °C up to 220 °C at which the device blew up.

*An improved experimental approach*

After multiple experiments of the kind described above, we found that sizable $I_D$ degradation only occurs after $I_G$ degradation is fully saturated, as clearly visible in Fig. 2. This suggests that we can study the degradation physics of $I_D$ and $R_D$ in a time efficient manner by redesigning the experiment to include an initial phase in which we quickly degrade $I_G$ to saturation while taking precautions to prevent device blow up. Once $I_G$ degradation is saturated, we can proceed to degrade $I_D$ using the approach described above. In this new initial phase, we can take advantage of the fact that $I_G$ degradation tends to occur fast and is rather temperature insensitive, while $I_D$ degradation evolves in a much more slow manner and it is temperature activated [30].

With these considerations, we designed a two-phase experiment with a flowchart that is shown in Fig. 6. In phase I, DC high-power electrical stress together with a very short temperature ramp from 50 °C to 220 °C is applied to the device under test. This is designed to fully saturate $I_G$ degradation without introducing any significant $I_D$ or $R_D$ degradation. In phase II, high-power stress is applied again with the base-plate temperature stepped up but the duration of each temperature step is much longer than above.

Results from phase I of a typical experiment are shown in Fig. 7. The device is stressed at $V_{DS}$ = 40 V and $I_{DQ}$ = 100 mA/mm with $T_{stress}$ raised from 50 °C to 220 °C in 20 °C steps. The stress time at each $T_{stress}$ level is 6 min. The device is completely detrapped by baking it at 250 °C for 7.5 h before $T_{stress}$ is brought to a new level. For enhanced effectiveness, the phase I ramp is repeated twice. This is denoted in the graph by labeling the data as 1st cycle or 2nd cycle. Indeed, we observe in Fig. 7b that a sudden increase of $I_{Goff}$ happens at the end of 1st cycle but during the 2nd cycle, $I_{Goff}$ remains at a relatively constant level. In Fig. 7a, we observe that the overall drain current degradation by the end of the 2nd cycle is very small, i.e., less than 4%. This shows that our goal of degrading $I_{Goff}$ without significantly degrading $I_{Dmax}$ at the same time is achieved.

Results from phase II of the same experiment are shown in Fig. 8. In Fig. 8a, $|I_{Goff}|$ stays at the saturated level produced in phase

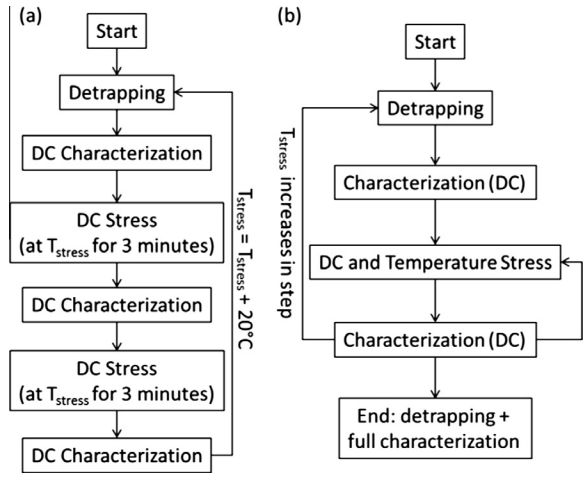


**Fig. 6.** Flowchart of improved step-temperatures stress experiment. (a) Phase I, designed to fully degrade $I_G$ without producing significant $I_D$ degradation and (b) phase II, designed to gradually degrade $I_D$ without any additional $I_G$ degradation.

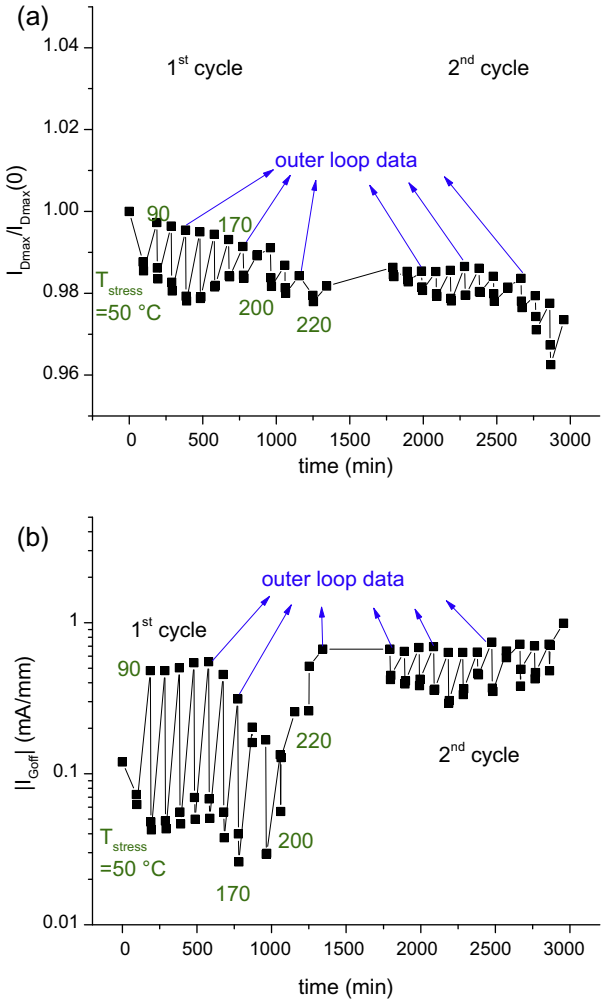


**Fig. 7.** Degradation of (a) $I_{Dmax}$ and (b) $|I_{Goff}|$ during phase I of a typical experiment under the improved experimental approach.

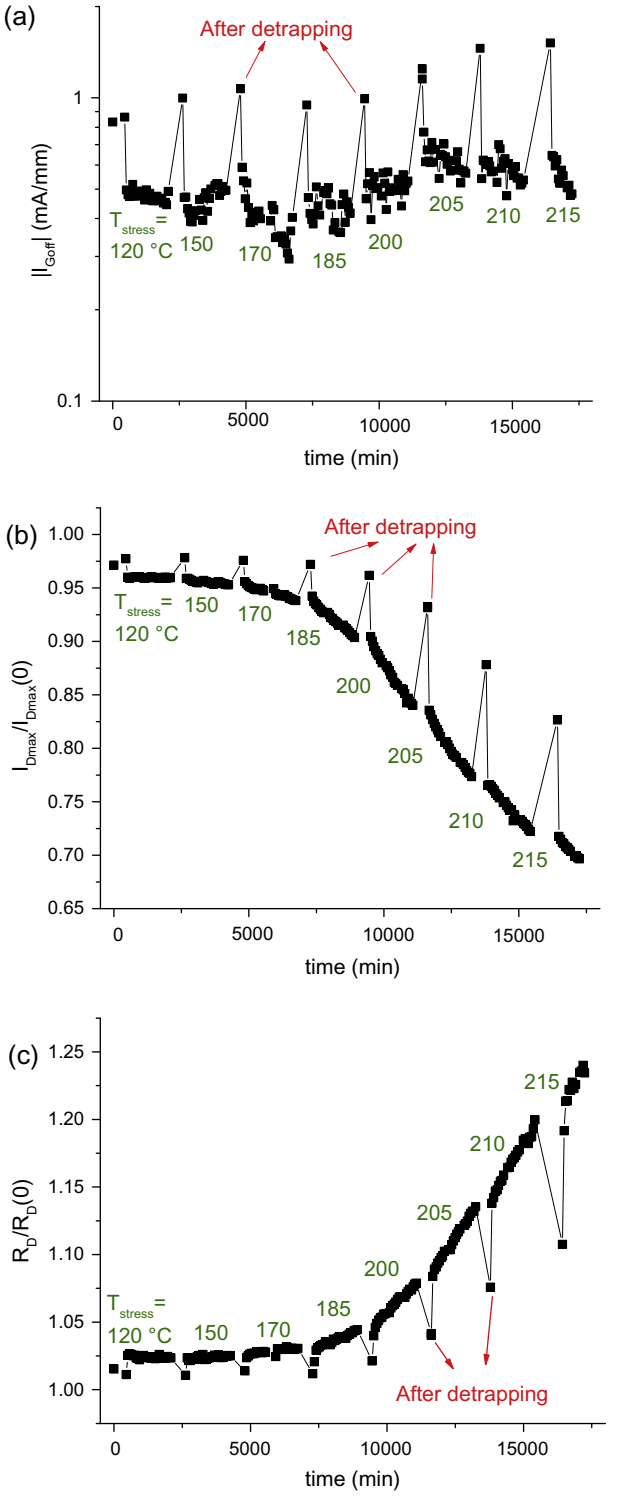


**Fig. 8.** Inner loop and outer loop results from phase II of 2-phase experiment ($T_{stress}$ = 120–215 °C): (a) $|I_{Goff}|$, (b) normalized $I_{Dmax}$ and (c) normalized $R_D$. Results from phase I are shown in Fig. 7. In this second phase, the device was stressed at $V_{DSQ}$ = 40 V and $I_{DQ}$ = 100 mA/mm and at a base temperature that increases from 120 °C up to 215 °C.

I while $I_{Dmax}$ (Fig. 8b) starts to decrease from $T_{stress}$ = 150 °C and ends up at 70% of its original value. The evolution of $R_D$ (Fig. 8c) correlates well with that of $I_{Dmax}$ and reaches an overall degradation of 25%. A clear thermally activated behavior is observed in the degradation rates of $I_D$ and $R_D$ in the outer loop. By fitting the experimental data with the Arrhenius law described previously, $E_a$ of 1.04 and 0.84 eV for $I_{Dmax}$ and $R_D$ respectively are obtained (Fig. 9). The two $E_a$'s differ by a small amount perhaps reflecting incomplete thermal detrapping.

In order to further improve the experiment to make it more effective and accurate in activation energy extraction, the stress time at each $T_{stress}$ level during phase II should probably be lengthened. Also, a more effective detrapping technique will also help. A possible one is the combination of thermal treatment and electric field bias. This will help detrap electrons through temperature independent tunneling processes [16,31].

## 4. Discussion

With this improved design of the two-phase experiment, several more experimental runs were performed on devices from the same technology. In devices that underwent enough total damage (>5%) so that the activation energy can be derived with some confidence, with only one exception, we have obtained activation energies for $I_{Dmax}$ between 0.83 and 1.04 eV. The anomalous case is one in which we obtained $E_a$ = 0.35 eV. This might reflect a different degradation mechanism being present in this device. $E_a$ for $R_D$ is similarly consistent. In devices that underwent enough degradation, we obtained values between 0.84 and 1 eV. One anomalous case yields $E_a$ = 2.4 eV. This is the same device that yielded an anomalous result for $E_a$ of $I_{Dmax}$.

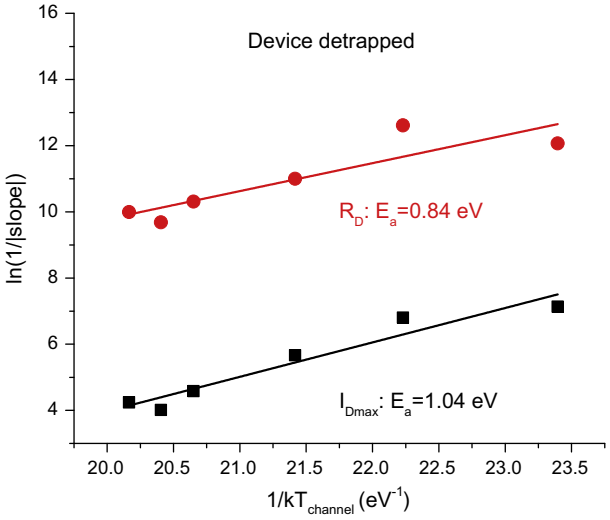


**Fig. 9.** Arrhenius plot of permanent $I_D$ and $R_D$ degradation rates extracted from outer loop data for the experiment of Fig. 8.

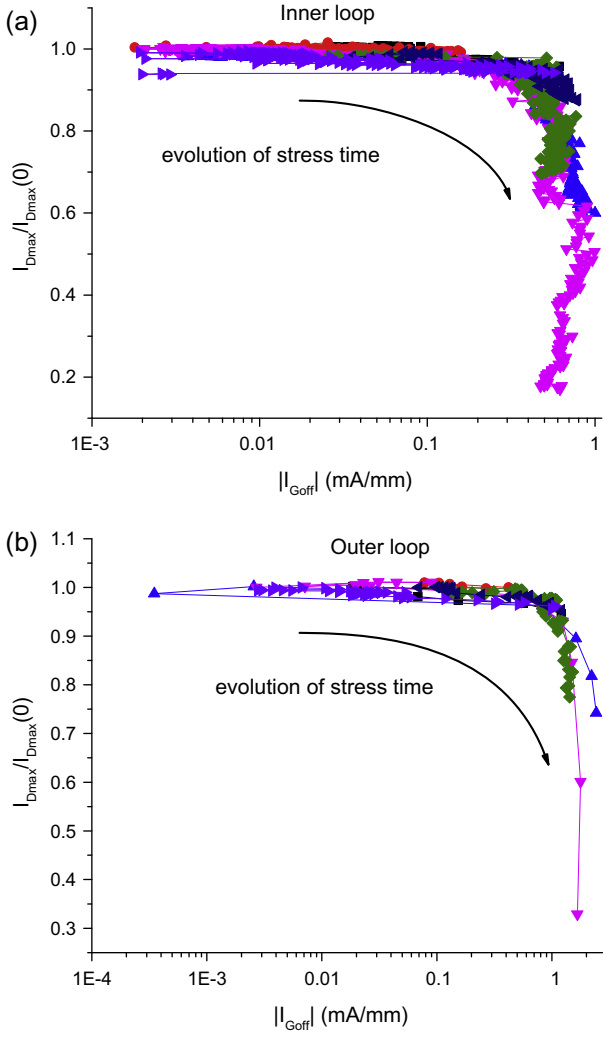


**Fig. 10.** Evolution of drain current degradation vs. gate current degradation of a number of devices (each color represents a different device) investigated in this study: (a) data measured within each temperature stress period (inner loop) and (b) data measured after detrapping steps (outer loop). (For interpretation of the references to color in this figure legend, the reader is referred to the web version of this article.)

A wide range of $E_a$'s obtained for different process technologies using a variety of techniques including the conventional accelerated life test method are reported in the literature and summarized in [10]. The reported values span from −0.15 eV to 2.47 eV. This large range probably reflects different process technologies, different level of process maturity, as well as the inherent difficulty of extracting activation energies. In addition, it might well be the case that the dominant degradation mechanism is not the same in all processes. Nevertheless, in experiments carried out on similar technologies as those performed here, $E_a$ for $I_{Dmax}$ obtained here closely matches values reported in the literature: 1.05 eV [32] and 1.12 eV [30].

An interesting aspect of our experiments is the consistent time-dependent pattern for $I_G$ and $I_D$ degradation that we have observed. Under high-power bias in step-temperature stress experiments, $I_G$ degradation occurs first and saturates. Only after this, $I_D$ and $R_D$ start to degrade without any further changes in $I_G$. Fig. 10 shows the correlation between $I_{Goff}$ and $I_{Dmax}$ degradation in a number of step-temperatures stress experiments on different devices under various high-power conditions. Both data from the inner loop and the outer loop are shown. A striking "universal" behavior confirms this picture for both permanent degradation and trapping-related degradation. This implies two different degradation mechanisms for $I_{Goff}$ and $I_{Dmax}$ that operate sequentially, just as observed under high-voltage stress in the OFF-state [15]. The recognition of a unified degradation pattern provides impetus to the development of a degradation model with lifetime predictive capabilities for a broad range of operating conditions.

## 5. Conclusions

In summary, we have studied the high-power degradation of GaN-on-SiC HEMTs. We have developed a new methodology that allows the extraction of the activation energy for permanent $I_D$ degradation through a new step-temperature stress methodology in a single device. We show that trapping is a major confounding factor in high-power reliability experiments. Under high-power stress we find that there are two sequential degradation mechanisms for $I_G$ and $I_D$. The activation energy for the permanent degradation of $I_D$ is between 0.83 eV and 1.04 eV in good agreement with separate reports on similar devices.

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